SCALABLE SYSTEM CHIP FOR COUPLING DATA BUS SYSTEMS

The invention relates to a scalable system chip for coupling at least two data bus systems.

Especially in automotive engineering, the problem arises that multiple data bus systems of different types are present in a vehicle. In order that data exchange may take place between the data bus systems of different types, so-called gateways are provided. Different designs of these gateways are known.

One option comprises the provision in a gateway of all the transceiver types that are suitable for the data bus systems provided in the vehicle. This means that, for every data bus, an assigned transceiver is provided, which, however, is in each case suitable only for a data bus type assigned to it.

The disadvantage of this solution is that different data bus systems may be provided in the vehicle, depending on the vehicle type, and, as a result, a gateway of this type would no longer be usable unreservedly simply as a result of even just one data bus type in the vehicle changing. A gateway of this kind is therefore unsuitable for, in particular, different vehicle types with differing data bus structures or differing data bus types.

It is an object of the invention to specify a scalable system chip for coupling at least two data bus systems, which exhibits the highest possible flexibility in respect of different data bus types used. This object is achieved in accordance with the invention by the features claimed in claim 1:

Scalable system chip for coupling at least two data bus systems, with at least one transceiver, integrated on the system chip, which is provided to create a coupling with a data bus of a first type, and with at least one controller, integrated on the system chip, to control at least one external transceiver, which is provided for coupling with a data bus of a second type.

Firstly, the scalable system chip in accordance with the invention is equipped with at least one transceiver, provided on the system chip and integrated on it, which is provided for a data bus type assigned to it. With this transceiver, data can be exchanged with this data bus type. Multiple transceivers may, of course, be integrated on the system chip, which are in each case then provided for a data bus type assigned to them.

In addition, the system chip is equipped with at least one controller, which is provided to control at least one external transceiver. This external transceiver is, in turn, provided for a particular data bus type. Multiple transceivers, which are in each case provided for a data bus type assigned to them, may be connected to the controller externally.

Owing to this architecture, the scalable system chip in accordance with the invention offers a high degree of flexibility, since the external transceivers can be provided as required and according to the data bus types encountered. For its part, the system chip is suitable for all situations and, as a result, can be used in any circumstances without having to be adapted.

Despite this flexibility, the system chip controls all transceivers, i.e. both those provided on the chip and those provided externally. As a result, optimum system reliability is guaranteed, despite the flexibility, since the control takes place virtually within a closed system.

As provided in accordance with an embodiment of the invention as claimed in claim 2, the system chip may advantageously operate together with an externally provided microcontroller, which processes at least parts of the send and/or receive protocols of the internal and external transceivers.

Since these send and/or receive protocols are, where applicable, implemented physically with different voltage levels, these signals may, as provided in accordance with a further embodiment of the invention as claimed in claim 4, advantageously be carried via the system chip that undertakes the corresponding voltage compensations.

In the event of a failure or of incorrect operation of the external microcontroller, the scalable chip can assume basic control tasks of the internal and external transceivers, as provided in accordance with an embodiment of the invention as claimed in claim 3. In a case of fault of this kind, the system chip can thereby nevertheless control all transceivers assigned to all the different data bus systems.

The invention will be further described with reference to an example of an embodiment shown in the drawing, to which, however, the invention is not restricted.

The Figure shows, in the form of a block circuit diagram, a scalable system chip 1 in accordance with the invention.

The system chip 1 is equipped with a first integrated transceiver 2, which is provided to create a coupling with an external data bus, of type A, which is not shown in the drawing.

The system chip 1 is further equipped with a second integrated transceiver 3 (optional), which is provided for coupling with a second external data bus type B.

Further provided in the system chip 1 is a controller 4, which controls and checks externally provided transceivers 8, 9 and 10 via control connections 5, 6 and 7. Each of these transceivers 8, 9 and 10 is provided for its own data bus type; as shown in the drawing, transceiver 8 is provided for a data bus type C, transceiver 9 for a data bus type D and transceiver 10 for another data bus type, which is here labeled with n, wherein C, D and n may also be of the same type.

The system basic chip 1 further operates together with an externally provided microcontroller 11, which the system basic chip 1 controls in respect of power supply (P), reset (R) and Interrupt (Int).

For the exchange of data between the system basic chip 1 and the microcontroller 11, a data bus D, which may be, for example, an SPI data bus, as known *per se*, is provided.

The provision and acceptance of data, sent and/or accepted by the internal transceivers 2 or 3 or the external transceivers 8, 9 or 10, may take place by means of the microcontroller 11. Provided for each transceiver are 2 lines, a send line and a receive line, which are not shown in the Figure. Since the transceivers 2, 3, 8, 9 and 10 and the microcontroller 11 can, where applicable, operate with different voltage levels, it is advantageous for these send and receive lines to be routed via the system chip 1, in which a corresponding voltage compensation is undertaken. Only the send and receive lines I/O between the microcontroller 11 and the system chip 1 are shown in the Figure; after any voltage conversion has been undertaken, these lead in the system chip to the transceivers 2 and 3 and, via the connections 5, 6 and 7, also to the externally provided transceivers 8, 9 and 10.

Further provided in the system chip 1 is a power supply unit 12, which can implement a power supply not just within the system chip 1, but also for the external transceivers 8, 9 and 10.

Owing to its architecture, the system chip 1 in accordance with the invention offers great flexibility since, on the one hand, the quantity of internal transceivers 2 and 3 can be adapted in line with anticipated requirements. In particular, however, the system chip 1 can be advantageously designed in such a way that it can drive a quantity of external transceivers 8, 9 or 10 that is sufficient in all cases. These external transceivers 8, 9 or 10 can be adapted in terms of their design in line with the particular requirements, i.e. the data bus types with which they exchange data. This adaptation is undertaken exclusively through the selection of suitable external transceivers, whereas the system chip 1 can itself remain unchanged.

It is advantageous hereby to provide the internal transceivers for those data bus types that are more or less always provided, and to provide the external transceivers for those data bus types that are only implemented in some cases.

Despite this high degree of flexibility, the system chip 1 offers a high degree of operational reliability, since, in the event of, for example, any hardware fault on the external microcontroller 11 or defective software of the microcontroller 11, it can nevertheless undertake certain basic control tasks (emergency operation) of both the internal and, as via the controller 4, the external transceivers.